Model Predictive-Based Voltage Balancing Control for Single-Phase Three-Level Inverters

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***Abstract*—Neutral-point (NP) voltage balance is critical for safe operation of single-phase three-level inverters. This issue can be overcome by selecting proper redundant small vectors. However, two voltage sensors are usually required to sample the split dc-link voltages. This letter proposes a model predictive-based voltage balancing method to reduce the usage of the voltage sensors (saving one voltage sensor). The required voltage information, which is essential for selecting the appropriate small vector, is obtained by comparing the current tracking errors. Consequently, the cost is reduced and the reliability is improved. A prototype is finally built to validate the feasibility and effectiveness of the proposed control method.**

***Index Terms*—Model predictive control, neutral-point (NP) voltage balance, single-phase three-level inverters, voltage sensors.**

I. Introduction

MULTILEVEL inverters generate various voltage levels at the output and have advantages of low harmonic waveforms, reduced voltage stress, and good electromagnetic compatibility in contrast to conditional two-level inverters [1, 2]. Therefore, they have received increased attention in both academia and industry for medium and high power applications [1-3]. Three-levels inverter, such as the neutral point clamped inverter [4] and T-type inverter [5], usually employs two series-connected dc capacitors to split the dc-link voltage into two. However, it suffers from the issue of dc-link capacitor voltage imbalance, which may cause harmonics in the synthesized output voltage and overvoltage across the switches.

Addressing this issue, from the viewpoint of hardware circuit, voltage balancing circuits, for examples, buck-boost converter [6, 7] or resonant switched-capacitor converter [8], are added to transfer energy between the series-connected dc capacitors. The balancing process and inversion are carried out without interference. The drawbacks are the increased cost, power losses, and control complexity. From the view of control, the neutral-point (NP) voltage can be balanced by adding zero-sequence voltage [9] or selecting the appropriate redundant switching state [5]. However, these methods need to know the voltages of the split dc-link capacitors. Hence, two voltage-sampling circuits are indispensable. Some three-level inverters with specific circuit structure have the function of self-voltage balancing [10, 11]. They require no extra voltage sensor or voltage balance circuit, and even no special attention is needed under the control process. In [10] a combined Cuk-Sepic converter is used as the front DC/DC circuit and its two output voltages are balanced automatically. Therefore, the inverter operates regardless of the NP voltage balance issue. In [11] a switched-capacitor (SC) block is used and the voltage balance is achieved because the split capacitors are connected in parallel when outputting the half dc-link voltage. This kind of voltage balance method is limited to specific circuit topologies and has a weak universality.

To overcome the cost of the balance circuit and the voltage sensor, this letter proposes a model predictive-based voltage balancing control for single-phase three-level inverters. It uses the current tracking error to obtain the information of which capacitor voltage is larger than the other. Then, the capacitor with larger voltage (with smaller voltage) will be discharged (charged). Then, the voltage balance will be realized without sampling both the split-capacitor voltages. The proposed control works at non-unity power factor. And experimental results verify the effectiveness of the proposed method.

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II. Mathematical Model

Fig. 1 shows the circuit structure of the investigated three level inverters. It can be a neutral-point-clamped (NPC) inverter [4] or a T-type inverter [5]. S_i (i=1, 2) is a single pole triple throw switch (SP3T) to present the switching state of each leg. And S_i=1 indicates the switch is connected to the positive bus voltage point P, S_i=0 the neutral point O, and S_i=-1 the negative bus voltage point N. The possible inverter output voltage vectors and the corresponding output voltage v_{ab} are listed in Table I.

From Fig. 1, the dynamic differential equations can be expressed as

$$L\frac{di_g}{dt} = v_{ab} - v_g \tag{1}$$

$$C\frac{dv_p}{dt} = i_{c1} \tag{2}$$

$$C\frac{dv_n}{dt} = i_{c2}. \tag{3}$$

Table I
Output Voltages Under Different Switching States

Vector	S_1	S_2	v_{ab}	i_{c1}	i_{c2}
$\boldsymbol{V_1}$ (PN), Large vector	1	-1	V_{dc}	$-i_g$	$-i_g$
$\boldsymbol{V_2}$ (PO), Small vector	1	0	v_p ($0.5V_{dc}$)	$-i_g$	0
$\boldsymbol{V_3}$ (PP), Zero vector	1	1	0	0	0
$\boldsymbol{V_4}$ (ON), Small vector	0	-1	v_n ($0.5V_{dc}$)	0	$-i_g$
$\boldsymbol{V_5}$ (OO), Zero vector	0	0	0	0	0
$\boldsymbol{V_6}$ (OP), Small vector	0	1	$-v_p$ ($-0.5V_{dc}$)	i_g	0
$\boldsymbol{V_7}$ (NN), Zero vector	-1	-1	0	0	0
$\boldsymbol{V_8}$ (NO), Small vector	-1	0	$-v_n$ ($-0.5V_{dc}$)	0	i_g
$\boldsymbol{V_9}$ (NP), Large vector	-1	1	$-V_{dc}$	i_g	i_g

Assuming the switching frequency is relatively high, (1) is discretized by using the forward Euler formula as follows,

$$i_g(k+1) = i_g(k) + \tfrac{L}{T_s}(v_{ab}(k) - v_g(k)) \quad (4)$$

where T_s is the switching period and L is the value of the ac filter inductor. A two-step prediction of the grid current is adopted in this letter to compensate the inevitable control delay [12]. Therefore, the two-step future grid current at the (k+2)th sampling instant is given as

$$i_g(k+2) = i_g(k+1) + \tfrac{L}{T_s}(v_{ab}(k+1) - v_g(k+1)). \quad (5)$$

Then, with the given grid current at (k+2)th instant, i.e., $i_g^*(k+2)$, the inverter output voltage during (k+1)th period is

$$v_{ab}^*(k+1) = \tfrac{L}{T_s}(i_g^*(k+2) - i_{gp}(k+1)) + v_g(k+1) \quad (6)$$

where $i_{gp}(k+1)$ is the predictive grid current at (k+1)th instant, which is obtained by applying the output voltage reference at kth instant $v_{ab}^*(k)$ into (4).

III. Proposed Model Predictive-Based Voltage Balancing Control

It's assumed that no over modulation happens and two vectors are used to synthesize v_{ab}^*, as shown in Fig. 2. It can be found that the small vector is always needed. Moreover, there exists a redundant small vector, which is the key to balance the NP voltage. To achieve this purpose, the voltage information of the split capacitors is critical when determining which small vector is used. Usually, two voltage sensors are needed to detect the voltages v_p and v_n. From the view of reducing cost and improving reliability of the system, less voltage sensors are expected. This is the original intention of the proposed MPC algorithm.

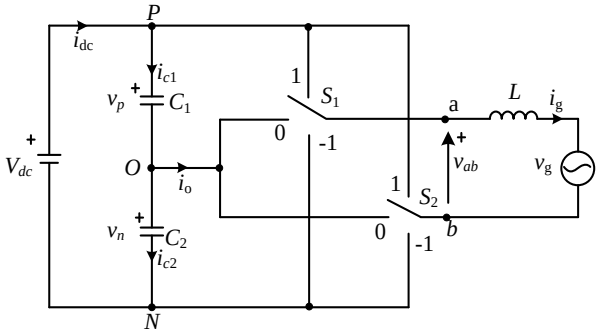

Fig. 1. Circuit structure of three level inverter.

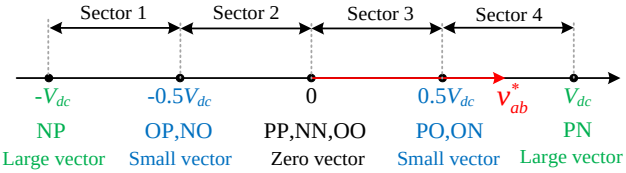

Fig. 2. Synthesizing the output voltage v_{ab}^*.

A. Analysis

Without loss of generality, the following assumptions have been made for later analysis:

1. The grid voltage and the grid current are positive. At (k-1)th instant, the NP voltage is not balanced any more and v_p=$0.5V_{dc}$-Δv.
2. During kth period, the small vector PO is selected and $i_g(k-1) = i_g^*(k-1) = i_{gp}(k-1)$. In addition, $v_{ab}^*(k-1)$ is given as

$$v_{ab}^*(k-1) = \tfrac{L}{T_s}\delta_i^*(k) + v_g(k-1). \quad (7)$$

where $\delta_i^*(k) = i_g^*(k) - i_g^*(k-1)$ is the expected current increment during kth period.

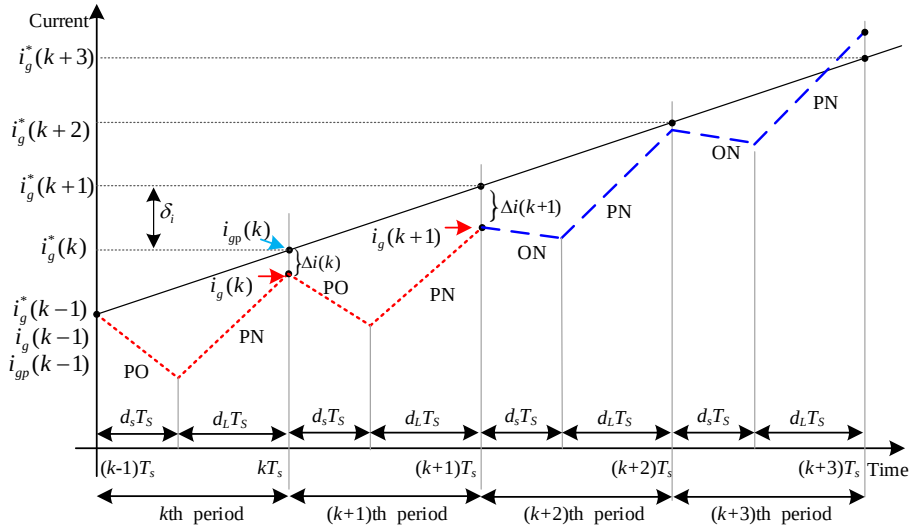

Fig. 3. Operating principle of the proposed MPC.

According to the hypothesis 1, the values of v_p and v_n can be expressed as

$$v_p = 0.5V_{dc} - \Delta v \tag{8}$$

$$v_n = 0.5V_{dc} + \Delta v \tag{9}$$

All duty ratios are calculated by considering a balanced NP voltage in the proposed control. Then, suppose v_{ab}^* is located in sector 4, duty ratios of the small vector (d_S) and the large vector (d_L) can be expressed as

$$d_S = 2 - \frac{v_{ab}^*}{0.5V_{dc}}, \tag{10}$$

$$d_L = \frac{v_{ab}^*}{0.5V_{dc}} - 1. \tag{11}$$

As a result of drifts of the NP voltage, the real inverter output voltage during kth period is

$$\begin{aligned} v_{ab}(k-1) &= d_s(k-1)v_p + d_L(k-1)V_{dc} \\ &= v_{ab}^*(k-1) - \Delta v d_s(k-1) \end{aligned}. \tag{12}$$

where

$$d_S(k-1) = 2 - \frac{v_{ab}^*(k-1)}{0.5V_{dc}}, \tag{13}$$

$$d_L(k-1) = \frac{v_{ab}^*(k-1)}{0.5V_{dc}} - 1. \tag{14}$$

The expected current increment during kth period is

$$\begin{aligned} \delta_i^*(k) &= i_g^*(k) - i_g(k-1) \\ &= \frac{T_s}{L}(v_{ab}^*(k-1) - v_g(k-1)) \end{aligned}. \tag{15}$$

The real current increment during kth period is

$$\begin{aligned} \delta_i(k) &= i_g(k) - i_g(k-1) \\ &= \frac{T_s}{L}(v_{ab}(k-1) - v_g(k-1)) \end{aligned}. \tag{16}$$

Subtracting (15) from (16) leads to

$$\begin{aligned} \Delta i(k) &= \delta_i^*(k) - \delta_i(k) \\ &= i_g^*(k) - i_g(k) \\ &= \frac{T_s}{L}(v_{ab}^*(k-1) - v_{ab}(k-1)) \end{aligned}. \tag{17}$$

According to (12), $\Delta i(k)$ can be represented as

$$\Delta i(k) = \frac{T_s \Delta v d_s(k-1)}{L}. \tag{18}$$

Then, the current error $e(k)$ is obtained as

$$e(k) = i_g^*(k) - i_g(k) = \Delta i(k). \tag{19}$$

i) If $e(k)>0$, $\Delta i(k)$ should be positive. According to (18), it can be concluded that Δv is positive and v_p is smaller than $0.5V_{dc}$. To balance the NP voltage, the other small vector ON (its voltage is v_n) will be applied in the coming (k+2)th and (k+3)th periods to discharge C_2. Then, the capacitor voltage v_p is prevented from being decreased further.

ii) If e(k)<0, $\Delta i(k)$ should be negative. It can be concluded that Δv is negative and v_p is larger than $0.5V_{dc}$. To balance the NP voltage, the same small vector PO should be applied in the coming (k+2)th and (k+3)th periods to discharge C_1.

Similarly, during the next step prediction, the error $e(k+2)$ will be calculated. If $e(k+2)>0$, it can be concluded that voltage provided by the used the small vector is smaller than its expected value $0.5V_{dc}$. Then, the other small vector should be applied in the coming two switching periods. Or, the same small vector will be employed. In other cases ($v_g>0$ and $i_g\leq 0$, $v_g\leq 0$ and $i_g>0$, and $v_g\leq 0$ and $i_g\leq 0$), similar analysis can be carried out. Fig. 4 shows the algorithm flow for selecting small vectors (supposing the selection is done every two switching periods).

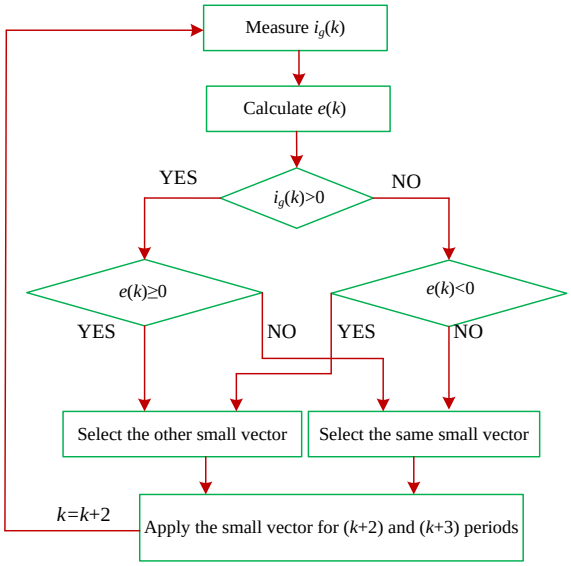

Fig. 4. Flowchart of the proposed MPC algorithm to select the small vectors.

B. Proof of the convergence

Subtracting (2) from (3) leads to

$$C\frac{d(v_n - v_p)}{dt} = i_{c2} - i_{c1} = -i_o. \tag{20}$$

When using the small vector ON or OP, (20) can be expressed as

$$C\frac{d\Delta v}{dt} = -i_o = -i_g T_s d_s. \tag{21}$$

And when using the small vector PO or NO, (20) can be expressed as

$$C\frac{d\Delta v}{dt} = -i_o = i_g T_s d_s. \tag{22}$$

Equations (21) and (22) can be generally expressed as

$$\begin{aligned} C\frac{d\Delta v}{dt} &= -sign(e(k)i_g(k))i_g T_s d_s \\ &= -sign(e(k))|i_g|T_s d_s \end{aligned}. \tag{23}$$

According to (18) and (19), $sign(e(k))$ can be simplified as

$$sign(e(k)) = sign(\frac{T_s \Delta v d_s(k-1)}{L}) = sign(\Delta v). \tag{24}$$

Substituting (24) into (23) leads to

$$C\frac{d\Delta v}{dt} = -sign(\Delta v)|i_g|T_s d_s \tag{25}$$

When Δv is positive/negative, the right part of (25) is negative/positive. Consequently, Δv converges to 0. In practice, $sign(e(k))$ is affected by the sampling error and delay, especially when $e(k)$ is very small. Therefore, the time interval of renewing the small vector should not be too short. In this letter, the selection is done every five switching periods.

IV. Experimental Results

To verify the theoretical analysis an experimental prototype of a T-type single-phase three-level grid-tied inverter, as shown in Fig. 5, was built and tested. It was designed for a 110 V_{rms} ac

output, a 250 V dc-input, and 500-W rated power. The switching frequency f_s is 20 kHz. L is 5mH, and C_1 and C_2 are electrolytic capacitors with the same value of 1 mF. The control algorithm of the converter is realized on a universal control board (Composed of digital signal processor TMS320F28335 and FPGA EP2C8T144C8N). Only one voltage sensor was used in the experiment to detect the dc-input voltage V_{dc}.

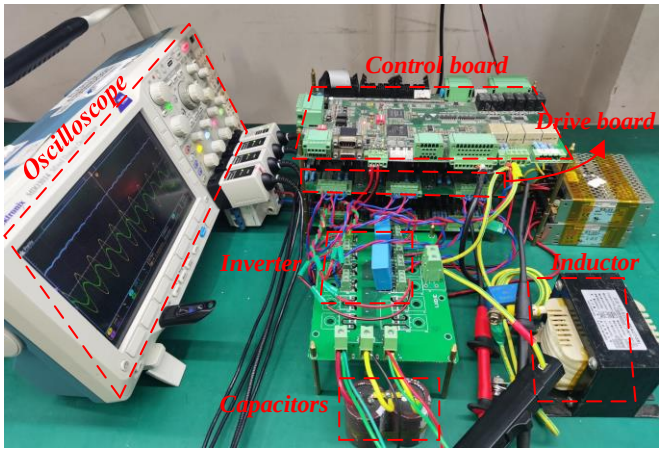

Fig. 5. Photo of the prototype.

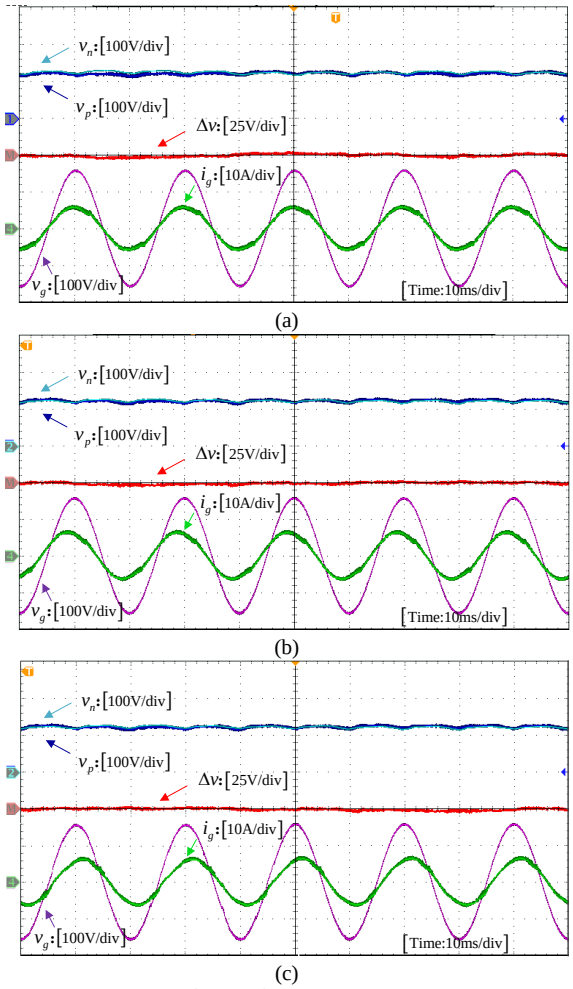

Fig. 6. Experimental waveforms of grid voltage v_g, grid current i_g, and split capacitor voltages v_p and v_n when the dc input voltage is 250 V. (a) Under unity power factor. (b) The grid current leads the grid voltage with $\pi/6$. (c) The grid current lags the grid voltage with $\pi/6$.

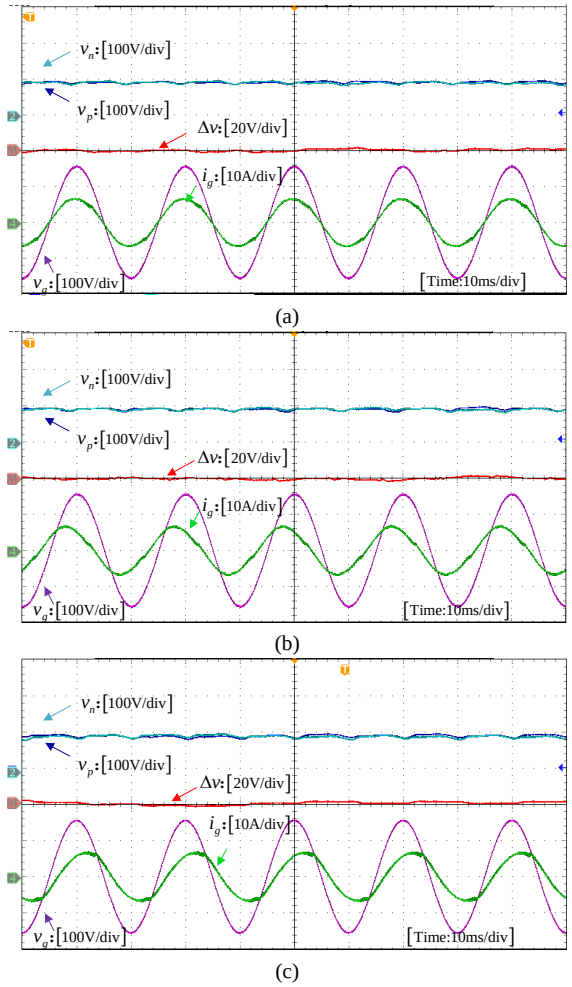

Fig. 7. Experimental waveforms of grid voltage v_g, grid current i_g, and split capacitor voltages v_p and v_n when the dc input voltage is 190 V. (a) Under unity power factor. (b) The grid current leads the grid voltage with $\pi/6$. (c) The grid current lags the grid voltage with $\pi/6$.

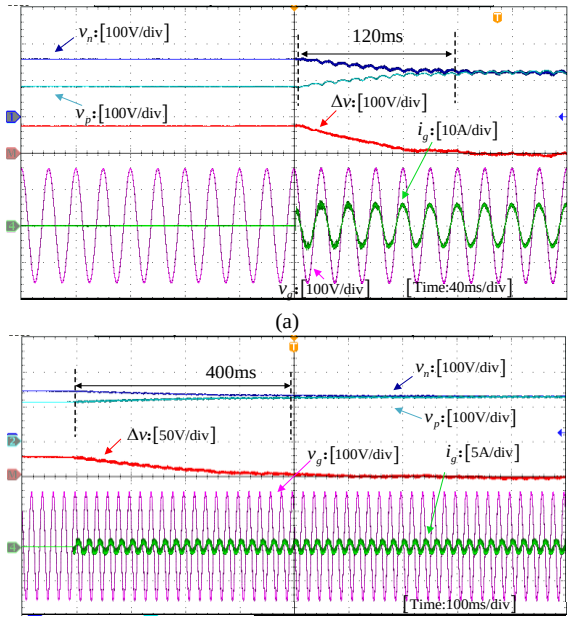

Fig. 8. Experimental transient waveforms of grid voltage v_g, grid current i_g, and split capacitor voltages v_p and v_n during start-up. (a) When the active power is 500 W. (b) When the active power is 0 W.

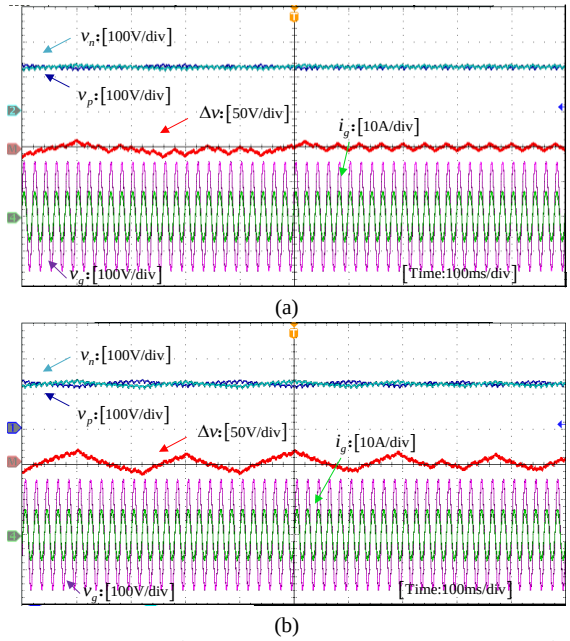

Fig. 9. Experimental waveforms when using mismatched parameters of the grid filter inductor L. (a) L is supposed to be 4 mH. (b) L is supposed to be 3mH.

Fig. 6 shows the experimental waveforms of split capacitor voltages v_n and v_p, the capacitor voltage difference Δv, the grid voltages v_g, and the grid current i_g. The dc input voltage is 250 V, i.e., the modulation index is 0.62. Fig. 6 shows the steady-state waveforms under unit power factor and non-unit power factor (the grid voltage lags/leads the grid current with $\pi/6$). As seen, in all conditions, the voltages v_p and v_n are almost equal and their difference Δv is within 5 V, which proves the effectiveness of the proposed balance method. It should be noted that a secondary pulsation phenomenon appears in the waveforms of split capacitor voltages v_n and v_p. This is caused by the inherent secondary pulsation power in single phase system. Fig. 7 shows the experimental waveforms when the dc input voltage is 190 V, i.e., the modulation index increases to 0.82. It can be found that the split capacitor voltages v_n and v_p can also be well balanced.

Fig. 8 shows the dynamic experimental waveforms when the active power is 500W and 0W. At the beginning, the converter is not synchronized and the voltages v_p and v_n are designed to be unbalanced on purpose. In both cases Δv is reduced to nearly zero after the system starts working. The only difference is that the convergence speed is faster when the active power is 500W.

Fig. 9 shows voltage balance performance when encountering the parameter drifts. The mismatched values of the grid filter inductor L are used in the algorithm on purpose. As seen, the voltages v_p and v_n can also be balanced. However, there exists large volage fluctuations (Δv is 10 V/20 V when L is supposed to be 4 mH/3 mH), which means the balance performance deteriorates.

V. Conclusion

In this letter, a new NP voltage balance method is proposed for single-phase three-level inverters based on model predictive control. The selection of the small vector is done by using the current error information. Consequently, single capacitor voltage measurements are voided, which improves the reliability of the system and reduces the cost. A test based on a T-type single-phase three-level inverter was carried out and the experimental results show that the voltage balance is well achieved under different operation cases. The proposed control idea can be extended to the other single phase three-level inverters. The subsequent researches will focus on applying the proposed control for the 3-phase system and improving the robustness against parametric variations.

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